

The new PICMG 1.3 specification – Bringing PCI Express to an SBC near you



By Michael Bowling, Trenton Technology Inc.

All too often committees create new embedded computing specifications with only a vague idea about what problem the specification is trying to solve. With PICMG 1.0 and 1.2 SBCs or System Host Boards (SHBs) and backplanes, many system designers are running into the inherent bandwidth limitations of parallel bus technology, especially when designing systems using the latest high-performance processors and chipsets. The PICMG 1.3 specification solves the bandwidth problem by replacing the SHB to backplane parallel bus interfaces with high-speed serial links. The specification corrects data bottlenecks, maintains backward compatibility with PCI and PCI-X option cards, provides additional power to the PICMG 1.3 edge connector, and offers advanced features such as IPMI, Serial ATA, USB, and Ethernet connections from the PICMG 1.3 SHB's edge connectors to the PICMG 1.3 backplane. The ubiquitous PICMG 1.0 system has long been a mainstay in the embedded computing industry due to its ability to support a large number of different option cards and system peripherals, while providing long MTBFs, fast MTTRs, long-life embedded component support, and flexible system designs. PICMG 1.3 continues that legacy while providing a faster system platform that maintains support for today's PCI/PCI-X option cards as well as PCI Express cards. The PICMG 1.3 specification replaces the PICMG 1.0 ISA/PCI bus combination with PCI Express and/or PCI/PCI-X interfaces to the backplane.

PICMG 1.3 overview

The PICMG 1.3 system host board interfaces to PCI Express peripherals on a backplane. Multiple PCI Express links to the backplane can operate at x1, x4, x8, or x16 depending on the capabilities of both the SHB and the backplane. Edge connectors A and B are the SHB's PCI Express links to the backplane. See Figure 1.

Today's PCI and PCI-X option cards can take advantage of the high-speed serial links, streamlined interconnects, and robust protocol that PCI Express offers in the PICMG 1.3 specification via PCI Express-to-PCI/PCI-X bridge chips on the backplane. The specification also accommodates an optional 32-bit PCI/PCI-X connection for supporting passive (such as no bridge) backplanes. The PCI/PCI-X clock rate between the SHB's optional connector D and the

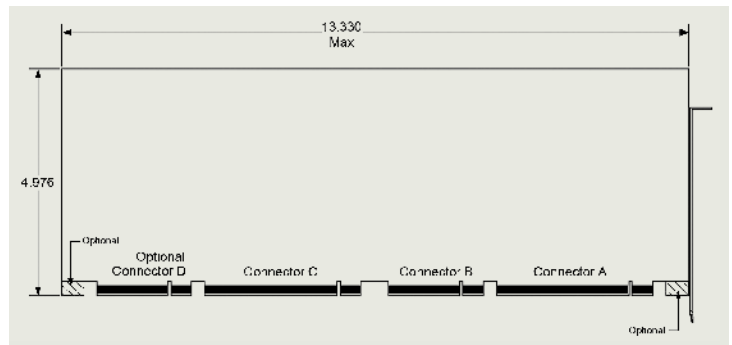


Figure 1

backplane can be 33 MHz, 66 MHz, 100 MHz, or 133 MHz, depending on the backplane's and the SHB's design.

SHB connector C contains extra edge connector contacts for additional power. The specification also features optional SHB to backplane interfaces for:

- SATA
- USB
- IPMB
- SMBUS
- Geographic addressing
- Power management

These features are available to the system designer to implement as needed. Figure 1 illustrates the full-size PICMG 1.3 SHB with all of the edge connectors defined. Figure 2 shows the half-size version.

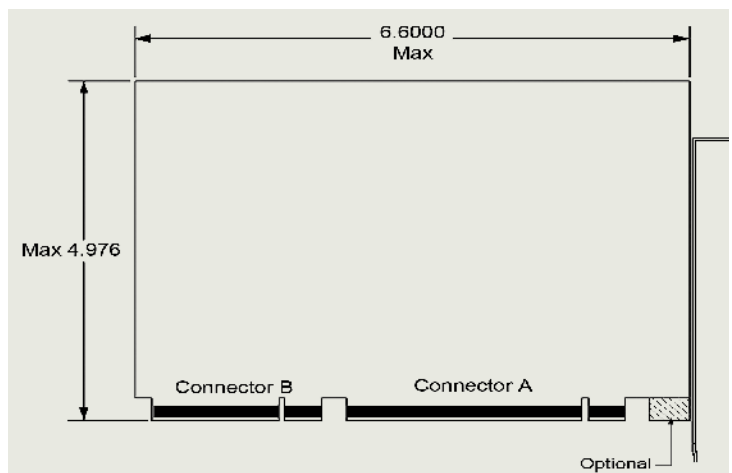


Figure 2

The PCI Express SHB to backplane configuration options offered by the PICMG 1.3 specification are designed to meet the needs of a wide variety of embedded computing applications. The flexibility built into the specification provides support for today's PCI and PCI-X option cards and the latest PCI Express card offerings. Provisions designed into the specification also provide future Advanced Switching option card support.

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PICMG 1.3 ratification timetable and summary

As I write this article, the key components of the PICMG 1.3 SHB and backplane specification are defined and complete. The final agreement on the specification's components among the twenty companies that make up the PICMG 1.3 Technical Subcommittee is in process. The subcommittee is planning final approval of the specification for the fall of 2004. PICMG 1.3 SHBs and backplanes will be available from multiple

embedded computing vendors in the late 2004 and early 2005 time frame.

These new, innovative embedded computing products will bring an improved level of PCI Express functionality and performance to industrial computing platforms. The PICMG 1.3 Technical Subcommittee has developed the PICMG 1.3 specification with maximum flexibility in mind. The specification's flexibility allows system designers to protect their organization's investment in PCI and PCI-X technology while taking advantage of the speed and increased bandwidth of PCI Express.

Michael Bowling is a design engineer and has been actively involved in designing board-level embedded computing products for a number of years. Trenton Technology is the draft editor for the PICMG 1.3 specification, and Michael is the lead writer for the specification. Michael holds a BS degree in computer engineering from the Georgia Institute of Technology and an MBA degree from Brenau University.

Trenton Technology Inc. is an Executive and founding member of the PCI Industrial Computer Manufacturers Group (PICMG) and one of the original developers of the PICMG 1.0 specification. Trenton designs and manufactures single board computers, system host boards, and backplanes for critical applied industrial and embedded applications such as telephony, imaging, instrumentation, control, and other environments that require performance, precision, and reliability. Visit www.TrentonTechnology.com for more details.

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