



CompactPCI™

**Short Form
Specification**

November 1, 1995

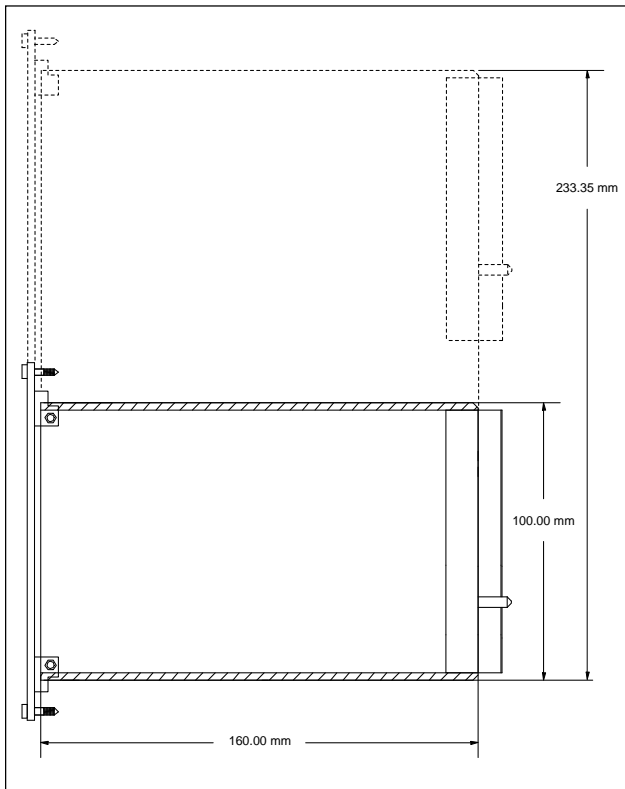


Figure 1. CompactPCI 3U and 6U format

Overview

This short form specification is a subset of the full CompactPCI specification, version 1.0 as approved by the PICMG. This document is meant as a guide for those considering CompactPCI, but is not a design document. Anyone wishing to design a system board, adapter board, or backplane for CompactPCI should obtain the full specification from PICMG™. A summary of the mezzanine definition defined in the supporting document *CompactPCI Mezzanine Applications* is also included.

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. CompactPCI uses industry standard mechanical components and high-performance connector technologies to provide a system optimized for rugged applications. CompactPCI is electrically compatible with the PCI Specification, allowing low-cost PCI chipsets to be utilized in a mechanical form factor suited for rugged environments.

Form Factor

The form factor defined for CompactPCI adapters is based upon the Eurocard industry standard. Both 3U (100.00 mm by 160.00 mm) and 6U (233.35 mm by 160.00 mm) board sizes are defined. See Figure 1 above.

The minimum form factor for CompactPCI is 100.00 mm by 160.00 mm (3U), 1.6 mm thick printed circuit board utilizing a 2 mm HM (IEC-1076) compatible connector for interfacing to the CompactPCI backplane.

CompactPCI accommodates extensions to the basic 3U form factor such as the 6U style. The double height board has the CompactPCI connector location designated as J1 on the lower portion of the board. A user defined connector area is also included.

Front Panels

CompactPCI adapter boards provide a front plate interface that is consistent with Eurocard packaging. A number of sources for front plates, mounting hardware, and ejector handles are available.

Single height 3U boards require only one ejector located on the bottom.

Double height 6U boards require two ejectors.

Systems

A **CompactPCI** system is composed of up to eight CompactPCI card locations with 20.32 mm (0.8 inch) board center-to-center spacing. The CompactPCI backplane consists of one System Slot, and up to seven Peripheral Slots.

The **System Slot** provides arbitration, clock distribution, and reset functions for all adapters on the bus. The System Slot is responsible for performing system initialization by managing each local adapter's IDSEL signal. Physically, the System Slot may be located at either end of the backplane.

The Peripheral Slots may contain simple adapters, intelligent slaves, or PCI bus masters.

Backplanes

Connector Orientation

The PCI interface connector orientation is illustrated as viewed from the front of the system chassis. Note that the System Slot may be located at either end of the backplane.

Other topologies besides the linear arrangement illustrated are allowed by CompactPCI. However, this specification and all backplane simulations have assumed a linear topology using 20.32 mm (.8 inch) board center-to-center spacing. Any other topology must be simulated to ensure compliance to the PCI specification.

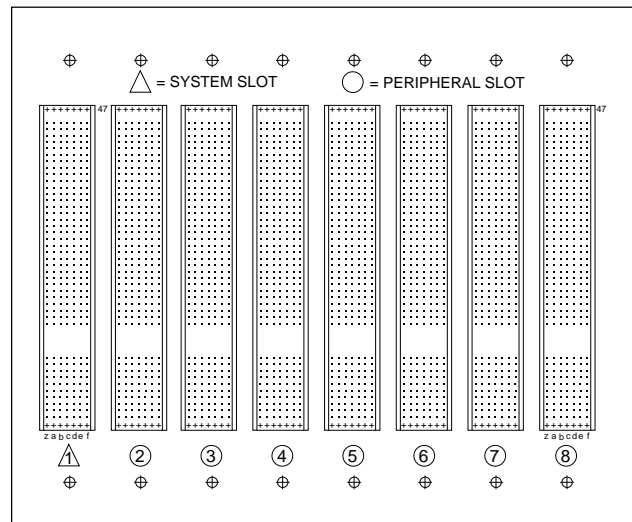


Figure 2. CompactPCI backplane

Slot Spacing

Slot spacing for CompactPCI is 20.32 mm (.8 inch). Backplanes must not have more than eight slots.

Physical Outline

The CompactPCI backplane connectors are designated P1, P2, P3, through P n , where n is the number of slots. For example, an eight slot backplane would designate the backplane connectors as P1 through P8.

Board slots on the backplane are designated 1, 2, 3, through n , where n is the number of slots. Slot numbering starts at the left end as viewed from the front.

Connector

The CompactPCI connector is a shielded, 2 mm-pitch, 7-row connector. This connector is currently manufactured by AMP, Framatome, and ERNI as a 2 mm, Hard Metric (2 mm HM) connector for telecommunication and backplane applications (IEC 917 and IEC 1076-4-101). Features of this connector include:

- Pin and socket interconnect mechanism
- Coding Mechanism providing positive keying
- Staggered make-break pin populations for optional hot swap capability
- Rear pin option for through-the-backplane I/O applications
- High density PCI capability
- High ground/signal ratio
- Shield for EMI/RFI protection

CompactPCI is defined as a 7 column by 47 row array of pins divided logically into two groups corresponding to the physical connector implementation. 32-bit PCI and connector keying is implemented on one connector (pins 1-25). An additional connector (pins 26-47) is defined for 64-bit transfers with a portion reserved for future use.

The CompactPCI connector utilizes guide lugs located on the adapter board connector to ensure correct polarized mating. Proper mating is further enhanced by the use of coding keys for +3.3 V or +5 V operation, with or without hot swap capability, to prevent incorrect installation of adapter boards.

Coding keys prevent inadvertent installation of a +5 V board in a +3.3 V system.

Hot Swap Capability

The CompactPCI specification accommodates a methodology for live insertion and removal of adapters into or out of an operating CompactPCI system. Adapters designated as “hot swap” provide a means for insertion and withdrawal while bus activity continues.

Additional work is ongoing to thoroughly define all aspects of hot swap specification. Future versions of this specification will incorporate additional details.

Connector Implementation

32-Bit PCI Signals

The 32-bit PCI signals are defined by rows 1-25 (*see Table 2*). On peripheral boards, one connector can be used to implement a 32-bit board, leaving rows 12-14 for connec-

tor keying. Rows 26-28 and 40-42 are primarily implemented on the System Slot board; rows 26-47 require the use of two connectors on System Slot boards.

Note: The number of System Slot signals utilized in rows 26-28 and 40-42 are dependent on the total number of slots implemented for any given CompactPCI system.

64-Bit Extensions

The additional signals for 64-bit PCI are represented by rows 26-47. All System Slot boards must implement rows 1-47; only 64-bit peripheral boards must implement rows 1-47.

Reserved Pins

Rows 40-42 contain the bused reserved (BRSV) signals. The BRSV signals in these rows are not to be used by system or adapter boards and are reserved for future expansion.

User Pins

Rows 43-47 contain user defined signals (USR). These signals are not bused and can be used for any user defined functions. If a backplane buses one or more of the USR signals to one or more slots, some form of notification should be provided to users (such as keying) to prevent damage to these signals on boards not designed for a bused application.

Power Pins

All CompactPCI connectors provide pins for +5V, +3.3V, +12V and -12V operating power. Additional power pins labeled +V(I/O) provide power for Universal adapters utilizing I/O buffers driving backplane signals that can operate from +5V or +3.3V. On these adapters, the PCI components I/O buffers shall be powered from V(I/O), not from +5V or +3.3V power pins.

Backplane pins labeled V(I/O) are connected to +5V on 5 V keyed systems and +3.3V on 3.3 V keyed systems. Alternatively, a separate V(I/O) power plane may be provided to supply 5 V or 3.3 V power.

Adapter Design Rules

Adapter board design is consistent with the design requirements for standard desktop PCI adapter boards as outlined in the PCI Specification. This section documents additional requirements and/or restrictions as needed.

Signal Termination

All bused PCI signals require a 10 Ω stub termination resistor located on the adapter at the CompactPCI connector interface. The signals that must be terminated are: AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, and RST#.

If used by an adapter, the following signals must also be terminated: INTA#, INTB#, INTC#, INTD#, SB0# , SDONE, AD32-AD63, C/BE4#-C/BE7#, REQ64#, ACK64#, and PAR64.

The following signals do not require a stub termination resistor: CLK, REQ#, GNT#, TDI, TDO, TCK, TMS, and TRST#.

The stub termination minimizes the effect of the stub on each adapter to the PCI backplane. The resistor is to be

47	GND	USR	USR	USR	USR	USR	GND
46	GND	USR	USR	USR	USR	USR	GND
45	GND	USR	USR	USR	USR	USR	GND
44	GND	USR	USR	USR	USR	USR	GND
43	GND	USR	USR	USR	USR	USR	GND
42	GND	BRSV	GND	PRST#	REQ6#	GNT6#	GND
41	GND	BRSV	BRSV	DEG#	GND	BRSV	GND
40	GND	BRSV	GND	FAL#	REQ5#	GNT5#	GND
39	GND	AD(35)	AD(34)	AD(33)	GND	AD(32)	GND
38	GND	AD(38)	GND	V(I/O)	AD(37)	AD(36)	GND
37	GND	AD(42)	AD(41)	AD(40)	GND	AD(39)	GND
36	GND	AD(45)	GND	V(I/O)	AD(44)	AD(43)	GND
35	GND	AD(49)	AD(48)	AD(47)	GND	AD(46)	GND
34	GND	AD(52)	GND	V(I/O)	AD(51)	AD(50)	GND
33	GND	AD(56)	AD(55)	AD(54)	GND	AD(53)	GND
32	GND	AD(59)	GND	V(I/O)	AD(58)	AD(57)	GND
31	GND	AD(63)	AD(62)	AD(61)	GND	AD(60)	GND
30	GND	C/BE(5)#	GND	V(I/O)	C/BE(4)#	PAR64	GND
29	GND	V(I/O)	BRSV	C/BE(7)#	GND	C/BE(6)#	GND
28	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
27	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
26	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
25	GND	5V	REQ64#	BRSV	3.3V	5V	GND
24	GND	AD(1)	5V	V(I/O)	AD(0)	ACK64#	GND
23	GND	3.3V	AD(4)	AD(3)	5V	AD(2)	GND
22	GND	AD(7)	GND	3.3V	AD(6)	AD(5)	GND
21	GND	3.3V	AD(9)	AD(8)	M66EN	C/BE(0)#	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
19	GND	3.3V	AD(15)	AD(14)	GND	AD(13)	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	KEY AREA						
11	GND	AD(18)	AD(17)	AD(16)	GND	C/BE(2)#	GND
10	GND	AD(21)	GND	3.3V	AD(20)	AD(19)	GND
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
6	GND	REQ#	GND	3.3V	CLK	AD(31)	GND
5	GND	BRSV	BRSV	RST#	GND	GNT#	GND
4	GND	BRSV	GND	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND
Pin	Z	A	B	C	D	E	F

Table 1. CompactPCI pinout

placed within 15.2 mm (0.6 inches) of the signal's connector pin. This length is to be included in the overall length of trace that is allowed for the signal

Peripheral adapters that drive REQ# should provide a series terminating resistor at the driver pin (not a stub termination resistor at the connector). On System Slot adapters, a series resistor (sized according to the requirements of the clock buffer) is assumed at the driver for the CLK signal provided to each slot. Each System Slot adapter's GNT# signal is also assumed to be series terminated at the driver with a resistor as required by the driving buffer technology.

Peripheral Adapter Signal Stub Length

Signal length for 32-bit signals (CompactPCI rows 1-25) must be less than or equal to 38.1 mm (1.5 inches). Signal length for 64-bit signals (CompactPCI connector pins 29-39) must be less than or equal to 50.8 mm (2.0 inches). These lengths are measured from the connector pin through the stub or series termination resistor to the PCI device pin.

These lengths are consistent with the PCI Specification requirements but also include the resistor in the total trace length. A maximum of one PCI load is allowed on any PCI signal.

System Slot Adapter Loading

The System Slot is allowed two PCI loads on each PCI signal to accommodate practical implementations of PCI-based CPU designs. The CompactPCI system modeling was performed with this requirement. The second load must not add more than 25.4 mm (1 inch) to the signal length for any PCI signal in addition to the 38.1 mm (1.5 inches) allowed for 32-bit PCI signals, or 50.8 mm (2.0 inches) allowed for 64-bit signals. Only one stub termination resistor is required per PCI signal on System Slot designs.

Peripheral Adapter PCI Clock Signal Length

On Peripheral Adapter boards, the PCI clock signal length must be 63.5 mm \pm 2.54 mm (2.5 inches \pm 0.1 inches), and is allowed to drive one load only on the adapter board.

Pullup Location

Pullup resistors required by the PCI specification are located on the System Slot adapter. The pull-up resistor, for those signals requiring a pull-up, must be placed on the in-board side of the stub termination resistor.

The System Slot adapter must provide a pull-up resistor for the REQ64# and ACK64# signals even if the System Slot adapter does not use these signals, as in the case of a 32-bit System Slot adapter. This requirement accommodates 64-bit adapters. They must see the signal REQ64# as false during reset to properly connect to the 32-bit PCI bus. The pull-up resistor also prevents floating REQ64# or ACK64# signals on 64-bit adapters.

J1 Shield Requirements

The J1 connector requires a shield to be loaded at row F on the adapter board. This shield covers the top of the IEC-1076 connector and helps to provide a low impedance return path for ground between the adapter board and the CompactPCI backplane. This is required for CompactPCI compliance and was used in the simulation modeling of the CompactPCI environment. Adapters that do not use this shield are not compliant and are not guaranteed to work in all CompactPCI system topologies.

The lower shield option that is provided for in the IEC-1076 connector is not required for CompactPCI adapters and should not be loaded.

Front Panel I/O Connector Recommendations

CompactPCI adapters should utilize metalized shell connectors for EMI/RFI protection. The shell should be electrically connected to the I/O plate through a low impedance path. The I/O plate is assumed to be connected to earth ground and isolated from logic ground. CompactPCI adapters should not connect earth ground (I/O plate) to logic ground used onboard.

Backplane Design Rules

CompactPCI defines a backplane environment that allows up to eight adapters without bridges. One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other 7 slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed.

Backplanes must provide separate power planes for +3.3 V, +5 V, and ground.

Clock Routing Requirements

A 2 ns maximum skew must be maintained between any two PCI components (not connector to connector) per PCI specification requirements. Adherence to backplane and adapter rules contained in this document help meet this requirement.

Parameter	Min.	Nom.	Max.	Units
Z ₀	-10%	65	+10%	ohms
R _{term}	-5%	10	+5%	ohms

Table 2. System Slot Adapter Loading

IDSEL Assignment

The PCI signal IDSEL is used to provide unique access to each slot for configuration purposes. By connecting one of the address lines AD31 through AD23 to each adapter's IDSEL pin (B9), a unique address for each adapter is provided during configuration cycles.

PCI devices on a System slot CPU board can be selected using lower ADxx lines in the range of AD11 to AD22.

REQ#/GNT# Assignment

The System Slot interfaces to seven pairs of REQx#/GNTx# pins called REQ0#-REQ6# and GNT0#-GNT6#. Each adapter slot interfaces to one pair of REQx#/GNTx# signals using pins called REQ# (A6) and GNT# (E5).

PCI Interrupt Binding

Interrupt binding of the BIOS setup program requires backplane assignments from the System Slot interrupt pins INTA#-INTD# to the adapter slot interrupts.

Backplane assignments rotate through adapter slots to provide a unique PCI interrupt to each adapter for the first four PCI connectors (assuming that each adapter drives just its INTA signal). Rotating interrupt assignments allows multiple PCI peripherals that drive only INTA# to utilize a different interrupt on the System Slot CPU without the need to share an interrupt with another PCI interface. Since multi-function PCI devices are allowed to drive more than one interrupt, shared interrupts may be required even within the first four adapter slots. In addition, the rotating pattern repeats itself after slot four, which also requires the sharing of an interrupt for slots that are four connectors apart (slots 2 and 6 for example).

CompactPCI Signal Additions

CompactPCI utilizes PCI signals as defined by the *PCI Local Bus Specification* with some additional signals. These additional signals do not affect the PCI signals but rather enhance system operation by providing push button reset, power supply status, System Slot identification, and legacy IDE interrupt support features. The additional signals defined are:

- Push Button Reset (PRST#)
- Power Supply Status (DEG#, FAL#)
- System Slot Identification (SYSEN#)
- Legacy IDE Interrupt Support

Power Distribution

Power is distributed in a CompactPCI system by utilizing a backplane. Each backplane must make provision for the standard regulated direct current (DC) supply voltages (+3.3, +5, +12, and -12VDC).

The backplane must provide power connectors for all of the supply voltages. One of two methods may be chosen:

- Power terminals may be located on the solder side of the backplane for external power sources.
- A DIN 41612 connector and solder side power terminals may be used for in-rack modular power supplies.

PCI Clock Distribution

The System Slot provides clock signals for all PCI peripherals in the system, including devices on the System Slot adapter. Peripheral adapters are provided clock signals via the CompactPCI backplane. A maximum skew of

2 ns is allowed in the system at 33 MHz between any PCI devices at the clock input of the integrated circuits.

Mezzanine Applications

CompactPCI 3U designs may be adapted into a mezzanine form factor for space constrained applications. The 32-bit portion of the connector pinout for CompactPCI is used for the interconnection between a host board and the mezzanine. With one core design layout, a 3U and mezzanine design can be created. The Mezzanine specification is a supporting document to the CompactPCI specification.

Typical uses for the CompactPCI mezzanine are in space constrained embedded applications such as STD, STD 32, G-64, Half-height ISA, and 3U Eurorack architectures.

CompactPCI Mezzanine Adaptation

The diagram illustrates the adaptation of a 3U CompactPCI design into a mezzanine form factor. A common design can be used for both applications. The mezzanine form factor is 51 mm by 135 mm.

+5 V/+3.3 V Mezzanine Keying

Mezzanine boards have mounting holes that are location keyed for +5 V or +3.3 V adapter board functionality. This mechanism prevents using +3.3 V mezzanine boards with +5 V base boards, and vice-versa. Universal mezzanine boards that can use either technology provide both key locations.

Mezzanine Connectors and Stand-off

Host Adapter Connector

The host adapter shall supply a 6 x 25 2 mm receptacle connector with a 3.55 mm (0.140 inch) body height. Rows 1-25 of the CompactPCI connector pinout are used for the mezzanine interface. Rows 12-14 are no-connect.

Mezzanine Connector

The mezzanine board incorporates a 2 mm header that also serves as a stand-off for the mezzanine. A 6 x 25 2 mm pin strip header is used for the electrical connection to the host adapter. CompactPCI limits the overall envelope of the mezzanine to be 12.7 mm (0.5 inch) above the mated surface of the host adapter.

Stand-off

Each CompactPCI Mezzanine interface shall be supplied with a nylon stand-off to secure the board and also to provide voltage keying information about the mezzanine.

Mezzanine Pin Assignment

The mezzanine pin assignment is identical to the first 25 rows of the CompactPCI backplane pin assignment (for 32-bit PCI) without the keying requirement.

Component Height Restrictions

The intention of the CompactPCI mezzanine is to create a small and low profile PCI expansion mechanism for host adapters. Due to this requirement, components used on the mezzanine interface and on the host interface underneath

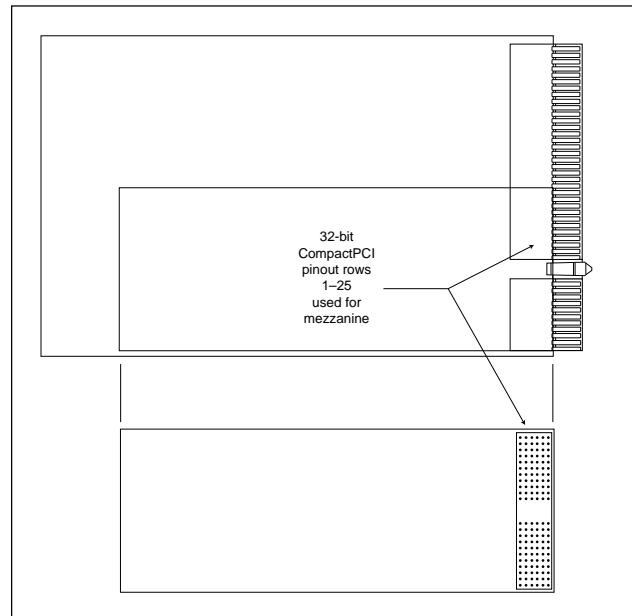


Figure 3. CompactPCI mezzanine pinout

the mezzanine are limited in component height above the surface of the mounted PCB.

Electrical Requirements

CompactPCI mezzanine interfaces are designed to the same electrical requirements as the full form factor board. The connector used for mezzanine applications is intended for use only as an add-on interconnect for one PCI load and does not meet the specifications for a bused topology such as multiple mezzanines in a stacked arrangement or other multi-card configuration.

Connector I/O

Each CompactPCI mezzanine adapter will have different connector I/O requirements. A connector I/O area is provided on the opposite side of the mezzanine as the CompactPCI connector. The connector may be loaded in this area and may be up to 5.03 mm (0.2 inches) in component height as allowed by the host adapter board.

Due to the varying requirements of standard interfaces (e.g., SCSI, Ethernet), it may not be possible to load the respective industry standard connector at this location. In these cases, the opposite surface of the board may be used, trading off additional assembly height for cabling ease. Manufacturers should clearly indicate the maximum assembly height when this approach is taken.

For a full copy of the *CompactPCI* specification, please contact the PCI Industrial Computer Manufacturers Group:
c/o Rogers Communications, 301 Edgewater Place, Suite 220, Wakefield, MA 01880, phone (617) 224-1100, FAX (617) 224-1239.